

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
13 January 2005 (13.01.2005)

PCT

(10) International Publication Number
WO 2005/004200 A2

- (51) International Patent Classification⁷: **H01L**
- (21) International Application Number:
PCT/US2004/019523
- (22) International Filing Date: 18 June 2004 (18.06.2004)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/482,527 25 June 2003 (25.06.2003) US
- (71) Applicant (for all designated States except US): **ADVANCED INTERCONNECT TECHNOLOGIES LIMITED** [MU/MU]; c/o Valmet (Mauritius) Limited, 608 St. James Court, St. Denis Street, Port Louis (MU).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **ISLAM, Shafidul** [US/US]; 3829 Lakedale Drive, Plano, TX 75025 (US). **SANTOS SAN ANTONIO, Romarico** [PH/ID]; Taman Duta Mas, Block A03-09, Batam Island 29433 (ID). **SUBAGIO, Anang** [ID/ID]; Taman Mediterania, Block GG2/No. 39C, Batam Island 29433 (ID).
- (74) Agent: **ROSENBLATT, Gregory, S.**; Wiggin & Dana LLP, One Century Tower, New Haven, CT 06508-1832 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

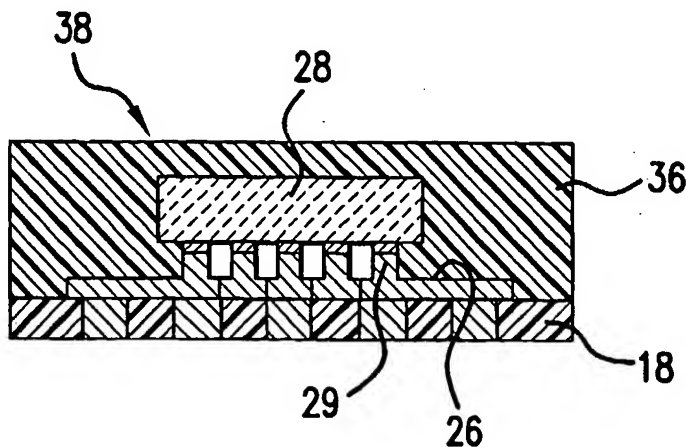
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: **LEAD FRAME ROUTED CHIP PADS FOR SEMICONDUCTOR PACKAGES**



(57) Abstract: A redistributed lead frame for use in molded plastic semiconductor package (38) is formed from an electrically conductive substrate by a sequential metal removal process. The process includes: (a) patterning a first side of an electrically conductive substrate to form an array of lands separated by channels, (b) disposing a first molding compound (18) within these channels, (c) patterning a second side of the electrically conductive substrate to form an array of chip attach sites (24) and routing circuits (26) electrically interconnecting the array of lands and the array of chip attached sites (24), (d) directly electrically interconnecting input/output pads on the at least one semiconductor device (28) to chip attach site members (24) of the array of chip attach sites (24), and (e) encapsulating the at least one

semiconductor device (28), the array of chip attach sites (24) and the routing circuits (26) with a second molding compound (36). This process is particularly suited for the manufacture of chip scale packages and very thin packages.